Antiphase Design for Balanced Oscillators

Liu Xiaoli*, Sheng Zhongxiang**, Law Choi Look**, Qian Cheng*** and Sun Zhongliang***

*S2-B4-C17, Comm. Research Lab. NTU, Singapore, 639798,exlliu@ntu.edu.sg.

**School of EEE, NTU, Singapore, ezxshen@ntu.edu.sg, ecllaw@ntu.edu.sg.

*** State Key Lab of Millimeter Waves, Southeast Univ. P.R.China, cqian@seu.edu.cn.

ABSTRACT

A novel general design method, which is based on S-parameters and suitable for MMIC and MEMS, has been developed for antiphase balanced oscillators in this paper. To demostrate the design method, a new type of interconnecting network is selected and a 7.0GHz balanced oscillator with antiphase dual outputs has been designed, fabricated and measured. difference of 180 degree between two outputs has been obtained. The measured results clearly verify the proposed design method.

***Keyword*:** Oscillator, MMIC.

1 INTRODUCTION

Balanced circuits are widely used to enhance circuit performance. The improvement of circuit performance relies heavily on the availability of antiphase signals, which is often the most difficult part of the circuit design. Traditionally, balanced signals are obtained by the use of passive baluns or active baluns; the latter are often complex, sensitive to the operating condition and have poor noise and linearity performance. Balanced oscillators providing antiphase outputs can eliminate the need for baluns. Several circuits generating antiphase oscillations have been reported in the literature [1-5]. In these oscillators, one approach is to couple the two oscillators in antiphase by using external resonators such as dielectric resonators [1], hairpin resonators [2], or microstrip patch resonators [3]. Another method is to use 180° phase shifter between the oscillators to force antiphase oscillations [4]. The third technique is to use a straight microstrip transmission line to connect two transistors [5], where the transmission line serves as a part of the resonant circuit. In summary, in all the above work, an interconnecting network with special parameters is inserted between two transistors. In this paper, a general technique for the design of balanced oscillator is presented. The technique is based on S-parameters of a general network which interconnects the two transistors. Such a general technique based on S-parameters does not appear to have been reported in the literature. Use of a general network offers additional flexibility in the design; for example, the general network can include a third port for injection-locking, or the interconnetcing network can include active devices. To demonstrate this general design technique, design and measurement results are presented for a microstrip antiphase balanced oscillator operating at 7.0 GHz.

2 BALANCED OSCILLATOR DESIGN TECHNIQUE

The schematic diagram of a balanced oscillator is shown in Fig.1. An interconnecting network between two identical transistors is described by its S-parameters. Because the interconnecting network is usually symmetric, and any losses in the interconnecting network can be treated as part of the load loss, the interconnecting network can be considered lossless and symmetric. As a result, $S_{12N} = S_{21N} = S_{KN}$, and $S_{11N} = S_{22N}$. Common source configuration is applied to both transistors to develop a negative conductance at the frequency of oscillation. Z_1 is optimized to increase the region of instability of the transistors. Z_2 is chosen to match the output impedance of the transistor to obtain maximum output power delivered to the loads. Under large signal condition, the input impedance of the transistors can be derived from Γ_g. When the interconnecting network is chosen to satisfy the following two conditions:

$$\Gamma_r * \Gamma_g = 1 \quad (1)$$

and

$$\Gamma_r = S_{11N} - S_{12N} \quad (2)$$

the phase relation at the two outputs of the interconnecting network can be solved to give

$$b_1 / b_2 = -1 \quad (3)$$

Eq. (3) implies that if the S-parameters of the interconnecting network satisfy (1) and (2), antiphase oscillations will be achieved.

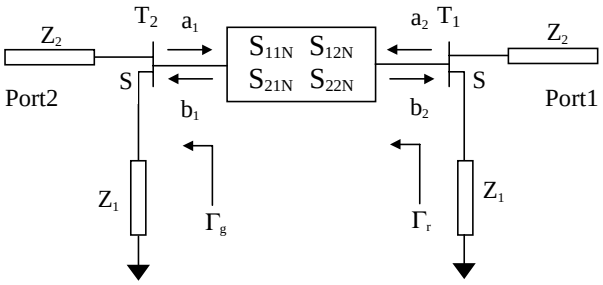

Fig. 1 Schematic diagram of a balanced oscillator incorporating a general interconnecting network

3 MEASUREMENT METHOD

The measurement is based on injection locking the balanced oscillator with a synthesized source in the vector network analyzer [6]. The network analyzer measures the phase of the reflection (S(1,1)) and transmission coefficients (S(2,1)) of the balanced oscillator. Denoting the phase of the oscillator signal at the injection port (port1) and the opposite port (port2) by θ_1 and θ_2 respectively, and the phase of the injection signal by θ_3, the phase relationship between the two outputs under locked conditions is given as follows:

$$\theta_2 - \theta_1 = (\theta_2 - \theta_3) - (\theta_1 - \theta_3) = \angle S(2,1) - \angle S(1,1)$$

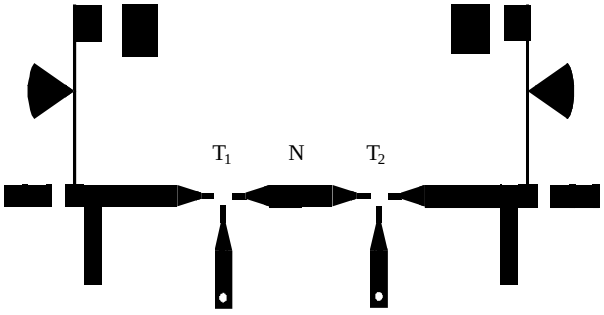

Fig. 2 Layout of the balanced oscillator including the bias network. N is the tapered – step interconnecting network

4 EXPERIMENT AND RESULTS

Based on the approach described above, a 7.0 GHz antiphase balanced oscillator has been designed. The circuit is fabricated on Taconic's substrate (TLX-0). The layout of the circuit is shown in Fig.2. A microstrip tapered-step is selected to work as the interconnection between two identical MESFETs (Agilent's ATF-26884). The tapered-step consists of two 100 Ohm microstrip lines, two tapers and one 50 Ohm microstrip line. The 50 Ohm section is 9 mm long, the tapered sections are 3 mm long, the 100 Ohm sections are 1.7 mm long. The measured spectrum shown in Fig. 3 indicates that a balanced oscillator operating at 6.999 GHz with output power 5.83 dBm is obtained. When the V_{DS} changes from 3V to 5V, the oscillating frequency varies from 6.96 GHz to 7.0 GHz. As shown in Fig.4, a nearly exact antiphase relationship between the two oscillator outputs is obtained. In conclusion, the measured results demonstrate excellent agreement with the new design method based on S - parameters.

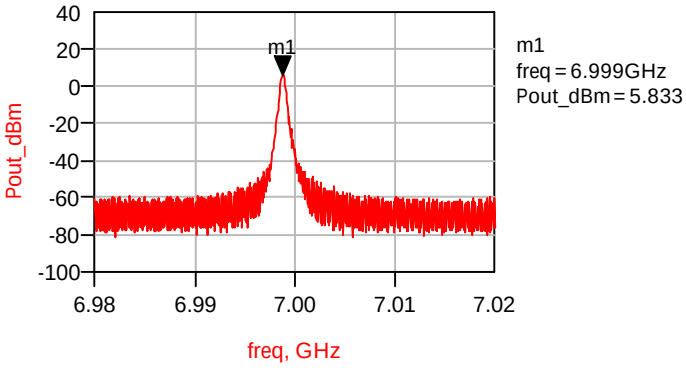

Fig. 3 Spectrum of the balanced oscillator output

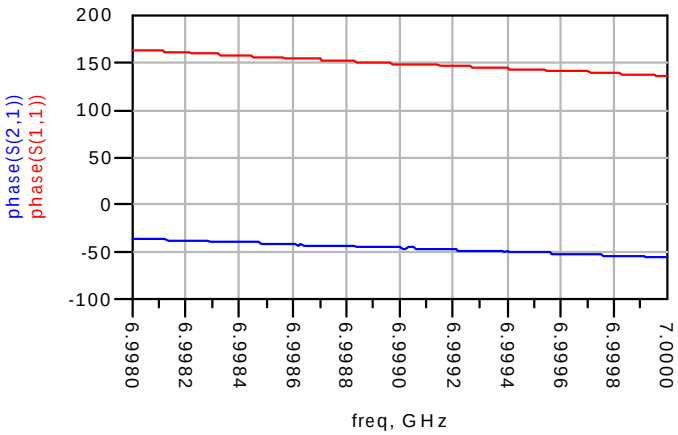

Fig. 4 Measured phase of the two output ports of the antiphase balanced oscillator

REFERENCES

[1] A.M.Pavio and M.Smith, "Push-push dielectric resonator oscillator" IEEE MTT-S Int. Microwave Symp. Dig., 1985, pp. 188-195.

[2] H.Yabuke, M.Sagawa and M.Makimoto, "Voltage controlled oscillators using miniaturized hairpin resonators" IEEE MTT-S Int. Microwave Symp. Dig., 1991, pp.1175-1178.

[3] J.Birkeland and T.Itoh, "Spatial power combining using push-pull FET oscillators with microstrip patch resonators" IEEE MTT-S Int. Microwave Symp. Dig., 1990, pp.1217-1220

[4] X.Zhou and A.S. Daryoush, "An injection locked push-pull oscillator at Ku-band" IEEE Microwave Guided Wave Lett., vol.3, Aug. 1993, pp. 244-246.

[5] K.S.Ang, M.J.Underhill and I.D.Robertson, "Balanced Monolithic Oscillators at K- and Ka-Band"

IEEE Trans. on Microwave Theory and Techniques, vol.48, No.2, Feb. 2000, pp187-193.

[6] A.P.S.Khanna and J.Obregon, “Direct measurement of the nonlinear MIC oscillator characteristics using injection locking polar diagram” IEEE MTT-S Int. Microwave Symp. Dig., 1983, pp.501-503.