Exact Simulation of LNAs Reduces Design Cycle Time

A 900 MHz design example illustrates the methods necessary to predict actual circuit performance using computer simulation

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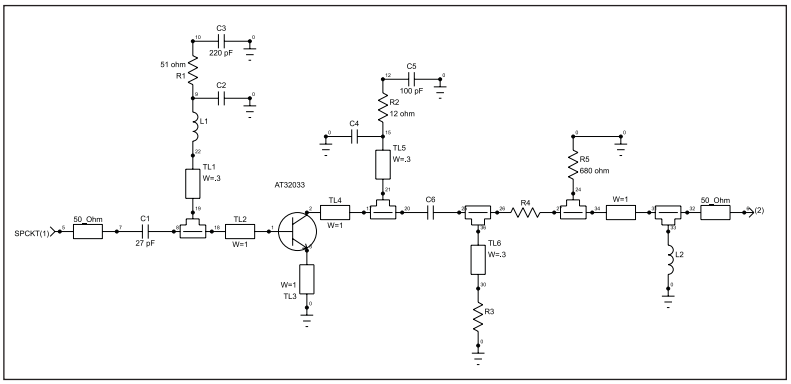
Simulated and measured data for 900MHz single-stage low noise amplifiers with <1.5:1 input VSWR are presented in this article. Excellent correlation is demonstrated between the simulation and measured data, and potential design and layout problems that may lead to poor circuit performance are discussed. A comparison of amplifier performance on FR4 and higher quality substrate is also given.



▲ **Accurate simulation can translate into faster design time.**

RF circuit design is still considered an iterative process in some circles. In fact many RF circuit designers accept circuit tuning or tweaking as part of the design process, often leading to multiple PCB iterations and increased design time. The ability to produce RF circuits with first time design success can provide a valuable competitive edge.

The specification of an LNA is strongly influenced by the intended application. Consideration must be given to performance, power consumption, linearity and cost. A compromise between these parameters is often necessary. Base station infrastructure applications usually have minimal power constraints so higher LNA power consumption can be tolerated to obtain better linearity. Battery powered equipment applications, however, usually demand low power operation.

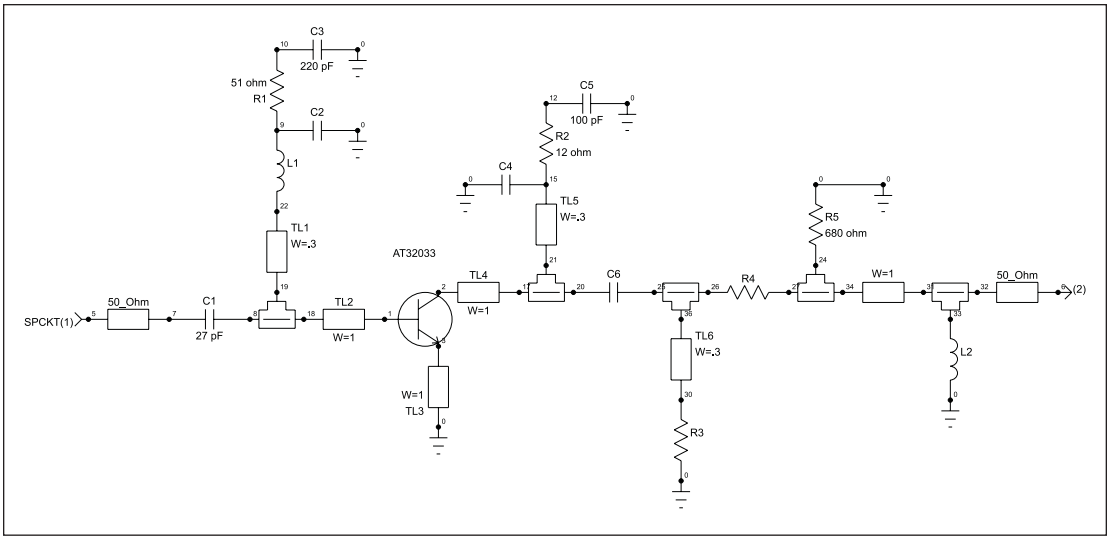
Component cost is another important consideration, usually forcing a compromise in other parameters such as noise figure and linearity. A low noise bipolar transistor is cheaper than a GaAs FET, but superior noise performance can be obtained from FET designs. Most portable wireless devices currently use silicon transistors. Component costs can be further reduced by using high impedance lines as inductive elements if real estate is available to accommodate the traces.

A transistor low noise amplifier design operating at 2.7 V, 2 mA will be presented in this article. Circuit performance on two different substrates will be compared. A high performance GaAs FET design biased for 2 V, 25 mA operation will also be presented for comparison.

Choose a device that can deliver the required noise performance. The noise figure listed on a device data-sheet is the optimum device noise figure for a 'typical' device when its input is terminated with the specified optimum noise match, Γ_{OPT}. This device noise figure does not include circuit losses, which can be high with low cost substrates such as FR4. You will obtain a poorer than specified noise figure from the device if your matching circuit presents a termination other than the optimum noise match

(Γ_{OPT}) to the device. The accurate measurement of noise figure has been detailed in the literature [1].

Bias your transistor or FET for the same operating condition as the S parameter data used in the simulation. The S parameter data is a representation of the device characteristics at a specific operating point. A different bias point for the same transistor can significantly alter the terminating impedances that should be presented to the device for optimum performance. Biasing a device at an operating point that is significantly different from that used for the S parameter data reduces the likelihood of good correlation between simulation and measured performance. If you design for unconditional stability using the S parameter data and then operate the device under different bias conditions your circuit may be unstable. Why risk this?



▲ **Figure 1. Simplified schematic of a 900 MHz transistor LNA.**

Most active devices that will be selected for use as low noise amplifiers in wireless applications will have gain, and the potential to oscillate, at frequencies much higher than the intended operating frequencies. The transistor used for two of the 900 MHz amplifiers discussed in this article has gain at 5 GHz. It is wise, and possible, to design for unconditional stability at all frequencies at which the device has gain. To this end, all microstrip discontinuities should be included in your circuit simulation. The effect of these step discontinuities will often be negligible at 900 MHz but can be significant at much higher frequencies.

Include the transistor mounting pads in your simulation. The mounting pad dimensions must be chosen to allow proper soldering of the device to the substrate. If your device has 0.5 mm wide leads, don't use a 0.3 mm line in your simulation to connect to the device. If you omit an appropriate mounting pad for the device, you will have poor correlation between your simulation and the measured circuit performance. Choose a pad topology that can be modeled with the available software tools. For these designs, Eagleware simulation and layout software was used. The circuit boards were fabricated using a T-tech Quick Circuit 5000 milling machine.

Include the mounting pads for passive components such as inductors, capacitors and resistors in your simulation. Include the step width discontinuities between the component pads and other traces in your simulation. A long microstrip line can be meandered to produce a more compact form factor. Include any bends in microstrip lines. If you follow the above design guidelines and simulate a design with unconditional stability, it is not likely that you will have any unpleasant surprises when you build your circuit.

Ideal passive components were used for the initial amplifier designs. Many passive component manufacturers provide S parameter data for their products. The ideal component models were then replaced with manufacturer's S parameter data. Microstrip component lengths were then adjusted to restore the desired performance if the component S parameter data caused a significant change to the circuit performance. Resistive loading may need to be increased if the real component data introduces a potential circuit instability ($k<1$). The manufacturer's S parameter data for the Murata GRM39 series chip capacitors, the Coilcraft 0603CS and 0805HT chip inductors and the ATC100A chip capacitors were used in the simulation of these amplifiers. All the resistors in these circuits were of the 0603 chip variety.

Be aware of the limitations of S parameter files. The S parameter data from some manufacturers is not very accurate and can lead to variations between simulated and measured performance. The manufacturer's data represents typical components. If you are using parts with a 5 percent tolerance you must expect to see some differences between simulated and measured results. Using statistical analysis, some components are only characterized over a limited frequency range. Most linear simulators will, however, extrapolate data beyond the frequency range included in the data files. If a component is characterized to 3 GHz, do not believe the results of your simulation at 5 GHz, where the accuracy of the extrapolated data is questionable. If your simula-

tion frequency range extends beyond the available S parameter data for the passive components, you can check circuit stability by using ideal component models and include parasitic elements [2].

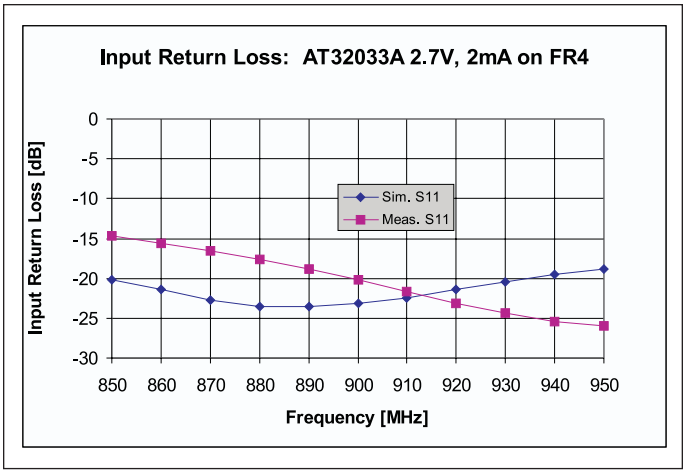
The Hewlett Packard AT32033 bipolar transistor was used for two amplifier designs, the first using 0.8 mm FR4 substrate and the other using the higher quality Taconic 60 mil RF-35 substrate. The manufacturers 2.7 V, 2 mA S parameters for this transistor were used. A simplified schematic diagram for these 900 MHz transistor low noise amplifiers is shown in Figure 1. Minor adjustments to component values and line lengths and widths were required to implement this circuit topology on the substrates with different thickness and dielectric constant. The actual base and collector bias circuits are not shown here. A Siemens BCR400 active bias chip was used to maintain the transistor's 2.7 V, 2 mA operating point. A single external resistor can be used with the BCR400 to set the transistor collector current.

For the sake of clarity the schematic in Figure 1 does not include the microstrip lines for component pads, the discontinuities due to microstrip bends or changes in line width or the effect of the via holes to ground. All of these effects were, however, included in the actual circuit simulations and are reflected in the simulated performance curves presented in this article.

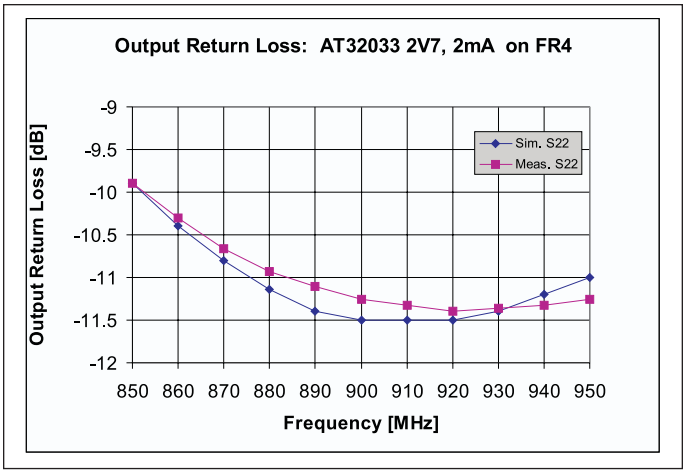
Capacitor C1 served as a DC blocking capacitor. The high impedance transmission line TL1 was connected in series with the lumped inductor L1 to provide input matching and a base bias injection point. Capacitor C2 provided low impedance at 900 MHz (close to short circuit in-band) while presenting a much higher impedance at very low (say <100 MHz) frequencies. Resistor R1 provides input loading to improve stability at very low frequencies. To avoid degrading the in-band circuit noise performance, the resistive loading at the device input is kept to a minimum. The value of C2 can, however, be selected to allow a small amount of resistive loading from R1 if this is required to improve device stability.

A small amount of inductance in the form of trace TL3 is included in series with the device emitter lead [3, 4]. This has the effect of moving the optimum noise match impedance (Γ_{OPT}) and the terminating impedance for optimum input match (S_{11}) closer together. When the device is matched for optimum noise performance, it is then also possible for the input match to be close to optimum.

The series transmission line TL4 was used as a matching element, along with series capacitor C6. Collector bias injection was via the high impedance transmission line



▲ **Figure 2a. Input return loss for the transistor LNA on FR4.**



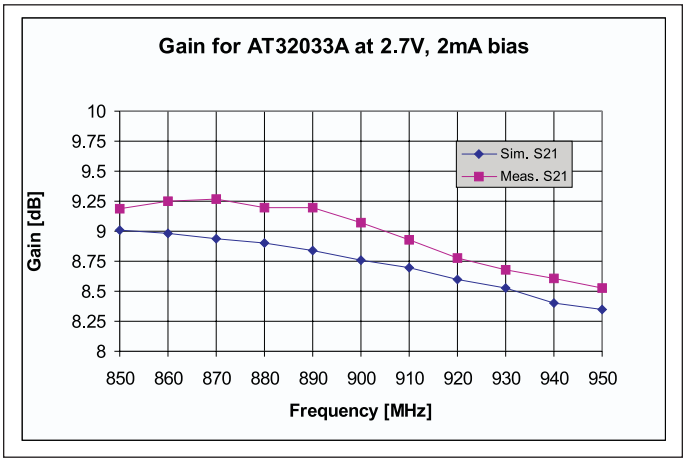
▲ **Figure 2b. Output return loss for the transistor LNA on FR4.**

TL5. There are four resistors used in the output matching circuit to ensure excellent device stability. Resistor R2 serves to enhances low frequency circuit stability. In higher current designs, the resistor must be constrained to a low value to prevent excessive power dissipation in this component. The shunt stub TL6 formed part of the output matching circuit. A small value series resistor R3 was included in this stub for enhanced amplifier stability.

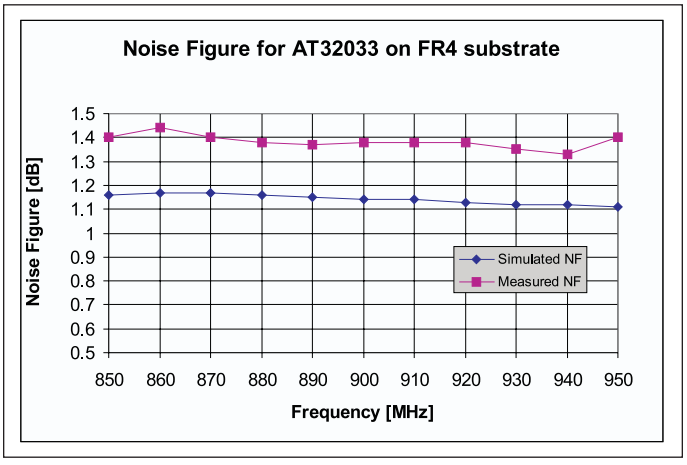
The value of the shunt resistor R5 is very high (680 ohms) and has minimal loading effect on the device while improving high frequency stability. The series resistor R4 has a low value (typically 2.2 to 6.8 ohms) to provide some circuit loading to enhance broadband amplifier stability. Although these resistors will have a very slight adverse effect on the amplifier noise figure and output compression point, this is a small price to pay for a highly stable circuit. The shunt inductor L2 formed part of the output matching network.

The amplifiers presented in this article were designed for operation over the 850 - 950 MHz frequency range. The design goal was an input VSWR of better than 1.5:1 with an output VSWR of at least 2.0:1. Unconditional stability at all frequencies at which device data was available was a requirement. The designs were optimized for minimum noise figure and maximum gain over the 850 - 950 MHz frequency range. No attempt was made to flatten the gain response of these single-stage amplifiers. Resistive feedback can be applied between the base and collector (gate and drain for a FET) of a transistor to flatten the gain response. There is usually a noise figure penalty associated with this. It is common to use this type of feedback in the latter stages of a multi-stage design to achieve a flat gain response without compromising the noise performance of the critical first stage.

The data for the LNA constructed on 0.8 mm FR4 substrate are presented in the following diagrams. The circuits presented in this article were constructed using the simulated component values, and no tuning, tweaking or component substitutions were made at all. Figure 2a shows the simulated and measured data for S_{11}. The input match was optimum at a slightly higher frequency than simulated, but the design requirement was met



▲ **Figure 3a. Gain for the transistor LNA on FR4.**

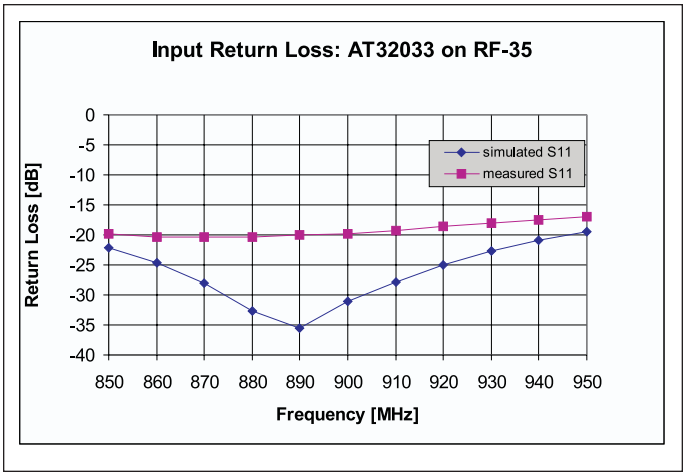


▲ **Figure 3b. Noise figure for the transistor LNA on FR4.**

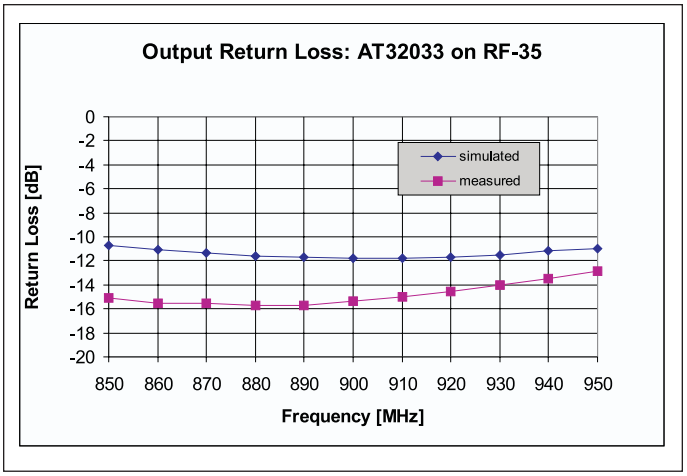
without circuit adjustment. A Monte Carlo analysis indicated that the measured performance was within the limits dictated by component tolerances. The data in Figure 2b indicate that the 10 dB output return loss requirement was easily met. The actual circuit gain displayed in Figure 3a was within 0.4 dB of the simulated response. The measured amplifier noise figure shown in Figure 3b was approximately 0.4 dB worse than predicted in the simulation. This measured noise figure was not predicted by statistical analysis. The high measured noise figure value could have been due to excessive substrate loss attributed to the use of many distributed elements on the FR4 PCB.

A similar amplifier circuit was fabricated on 60 mil RF-35 Taconic substrate for comparison. The circuit topology shown in Figure 1 was also used for this amplifier. The simulated and measured results for S_{11} and S_{22} are shown in Figures 4a and 4b. The design requirement for these parameters was easily met and the measured results were within the limits predicted by statistical means. The similar measured and simulated circuit gain responses are graphed in Figure 5a. The noise figure results in Figure 5b indicate that the actual circuit noise figure was within 0.2 dB of the simulated value. It can be seen from the data above that there was good correlation between simulated and measured performance for all of the above parameters. From the above data it seems that the simulated noise figure value was slightly optimistic, and the simulation was not entirely successful at predicting the noise performance on the FR4 material. The electrical parameters of FR4 are poorly controlled during manufacture. A nominal value of $\varepsilon_r = 4.7$ and loss tangent = 0.025 were used in the simulation. Substantially changing these parameters in the simulation could not, however, predict the actual measured circuit noise performance. FR4 PCB material can also exhibit anisotropy with respect to dielectric constant and this may have adversely influenced the meandered microstrip components.

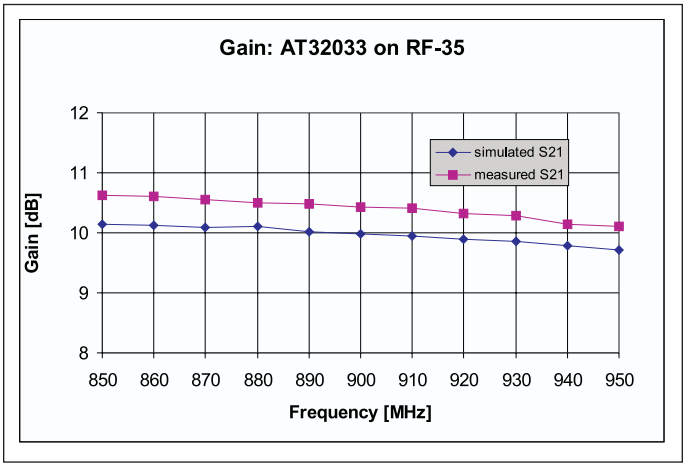
The transistor was conjugately matched in the above circuits, with no attempt to provide the optimum power termination to the device output. For the FR4 design, the P_{1dB} point was measured to be –3.4 dBm with an output IP_3 of +10.3 dBm. The circuit built on RF-35 substrate had a P_{1dB} of –2.7 dBm and an IP_3 of +16 dBm. The latter IP_3 result was tested numerous times and appears to be correct. This unusually high value for IP_3 has been previously reported with this device [5] and seems to be matching circuit dependent. The design described in [5] achieved similar noise performance to the FR4 design presented here,



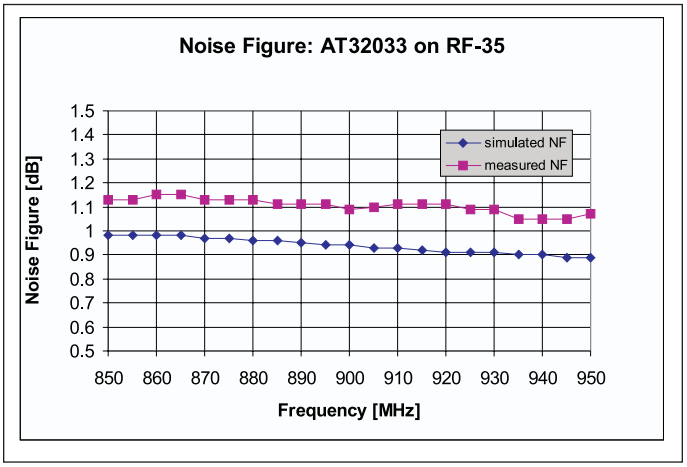
▲ **Figure 4a. Input return loss for the transistor LNA on RF-35 substrate.**



▲ **Figure 4b. Output return loss for the transistor LNA on RF-35 substrate.**



▲ **Figure 5a. Gain for the transistor LNA on RF-35 substrate.**



▲ **Figure 5b. Noise figure for the transistor LNA on RF-35 substrate.**

but with an input return loss of approximately 7.5 dB at 900 MHz.

The AT32033 has a good noise figure for a silicon transistor but a GaAs FET or HEMT is required for amplifiers with substantially better than 1 dB noise figure. The Celeritek CFB0301 GaAs FET was used in the amplifier circuit configuration shown in Figure 6. No chip inductors were used in the design and all inductive elements were implemented as high impedance lines on the 0.060 inch Taconic RF-35 material. Capacitor C1 served as a DC block with input matching provided by traces TL1 and TL2. Note that the FET package has two source leads and traces TL3 and TL4 are each connected to one of those leads. Remember to include via holes in your simulation as these add inductance to the source traces. Output resistive loading to ensure device stability is provided by the low value (2.2 - 6.8 ohm) resistors R2 and R5. The high value shunt resistor R4 does improve high frequency stability with minimal degradation of the output power compression point. Capacitors C2, C3 and traces TL5, TL6, TL7 and TL8 formed the remainder of the output matching network.

The manufacturer's 2 V, 25 mA S parameter data were used for this design. Ideally, any design should have noise and S parameter data available at the same bias point. This allows the designer to simulate all parameters of the design, including noise-figure and stability k-factor, and have confidence that the actual circuit will perform as simulated. Regrettably, the manufacturer of the CFB0301 has provided noise data and S parameter data at different bias conditions. The available manufacturers data, the 2 V, 25 mA S parameter data and the 4 V, 30 mA noise data, were used for this design.

The simulated circuit was designed for unconditional stability using the S parameter data and the amplifier was biased for 2 V, 25 mA operation to ensure stable operation. A dual supply was used for this amplifier, with a gate bias voltage of approximately –0.79 V resulting in 25 mA drain current. It was understood that there could be a discrepancy between the simulated and mea-

sured noise figure due to the different bias conditions for the noise data and the actual circuit.

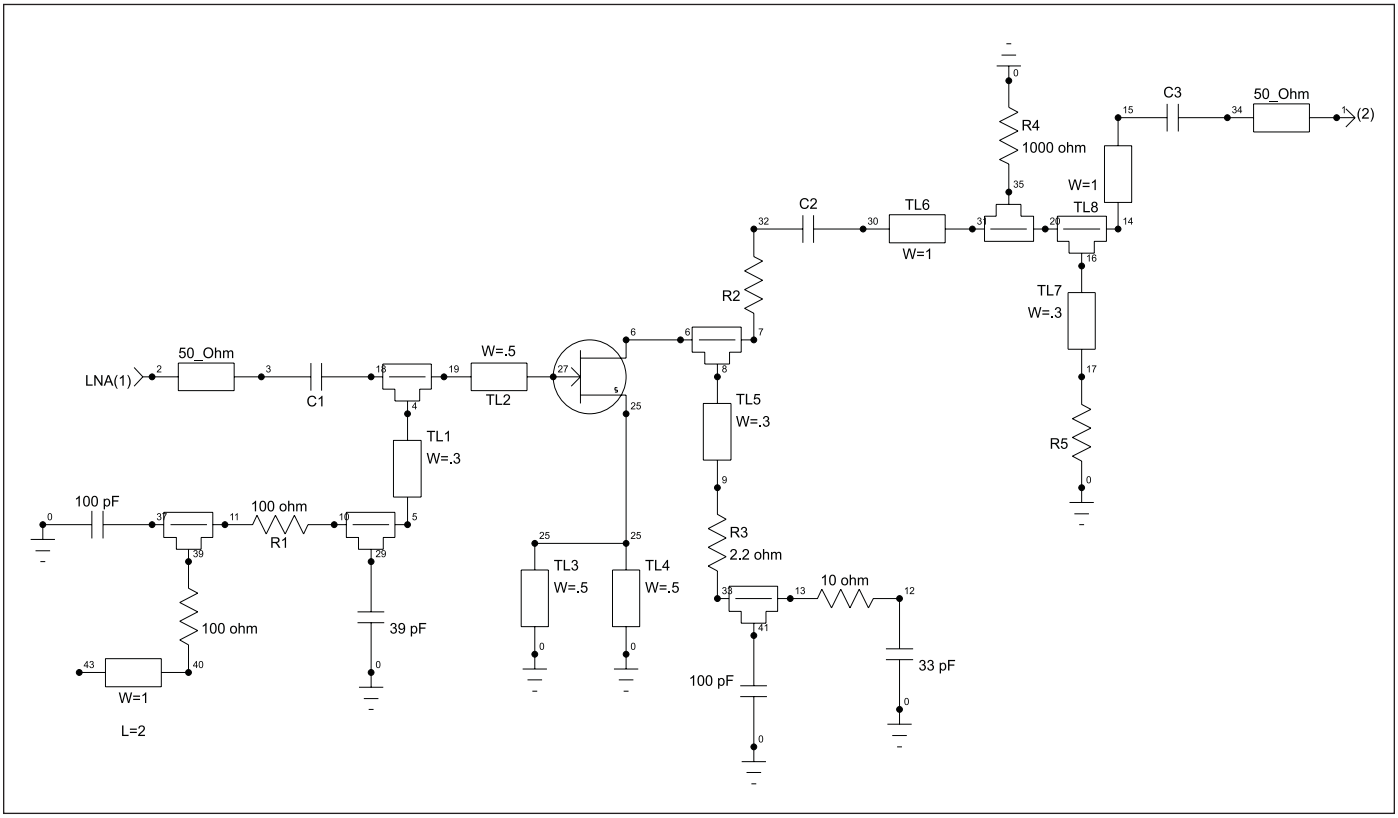
The simulated and measured input and output return loss data for this GaAs amplifier design are presented in Figures 7a and 7b. The input return loss was better than -15 dB and output return loss better than –10 dB over the 850 - 950 MHz frequency range. The output return loss response is within the limits predicted by a Monte Carlo analysis of the circuit. The amplifier gain responses recorded in Figure 8a demonstrate very good correlation between simulated and measured performance.

A plot of the amplifier noise figure is given in Figure 8b. The amplifier noise figure was measured as less than 0.46 dB over the 850 - 950MHz frequency range. This is an excellent result given that the CFB0301 device has an optimum noise figure of 0.4 dB at these frequencies. The simulated noise figure prediction varied from 0.61 dB to 0.64 dB over this frequency range. This was clearly pessimistic and is not surprising given that the noise figure prediction was based on data taken at a completely different bias condition (4 V, 30 mA). We were fortunate that the actual circuit noise figure was better than predicted. It is highly desirable to have device noise and S parameter data at the same bias point to obtain good correlation between predicted and measured performance. For interest, the circuit noise figure was recorded over a wider span and found to be <0.6 dB over the 700 - 1200MHz frequency range. All noise figure measurements presented here were measured in a screened room using an HP346A noise source and an HP8970A noise figure meter. The amplifier's output power compression point (P_{1dB}) was determined to be +13.2 dBm. The third order intercept point was found to be +25.1 dBm using a two-tone test at 900 MHz.

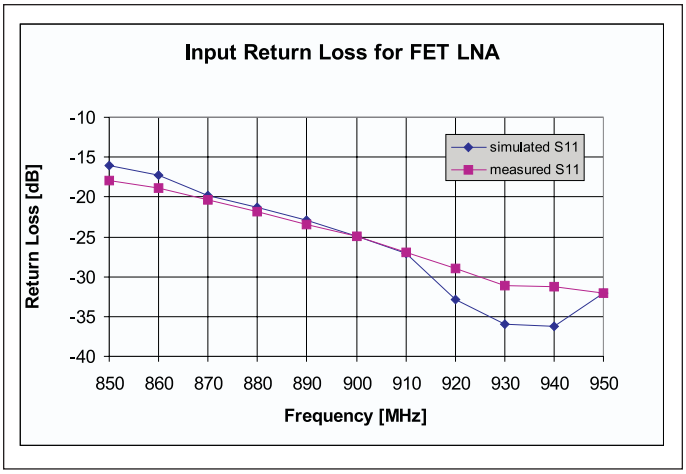
The simulated and measured performance for three different amplifiers has been compared in this presentation. By following a few simple guidelines it is possible to produce high performance LNAs without multiple design iterations:

- Choose a device that is appropriate for the intended application. Silicon transistors can be low cost but a FET can offer superior noise performance.
- The use of emitter or source feedback in the amplifier circuit allows the designer to simultaneously obtain good noise performance and a good input match.
- Avoid unintentional coupling between microstrip elements in the circuit layout.
- Resistive loading for device stabilization should be applied largely to the device output to avoiding degrading the circuit noise performance.
- Include all microstrip discontinuities, including component pads, in your circuit simulation. This will allow accurate evaluation of the amplifier's high frequency stability.

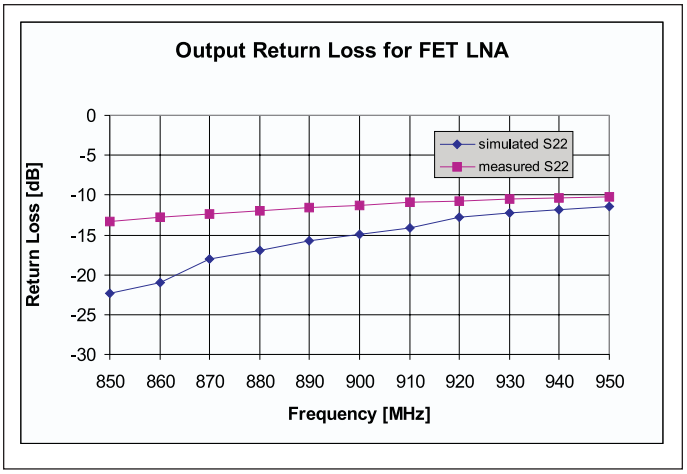
The circuit modeling techniques presented in this



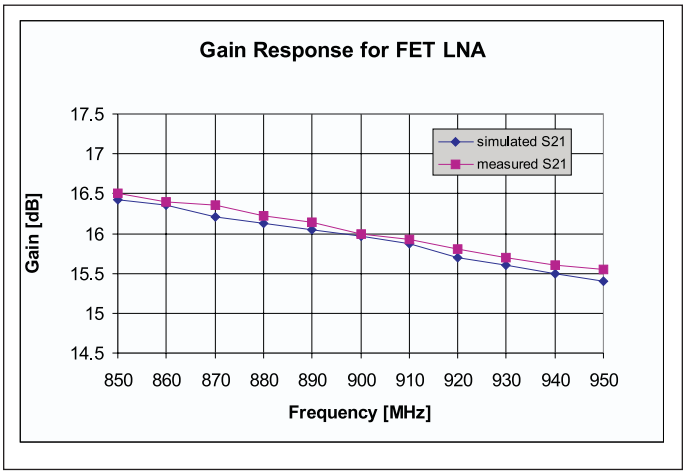
▲ **Figure 6. Simplified schematic diagram for the FET LNA.**



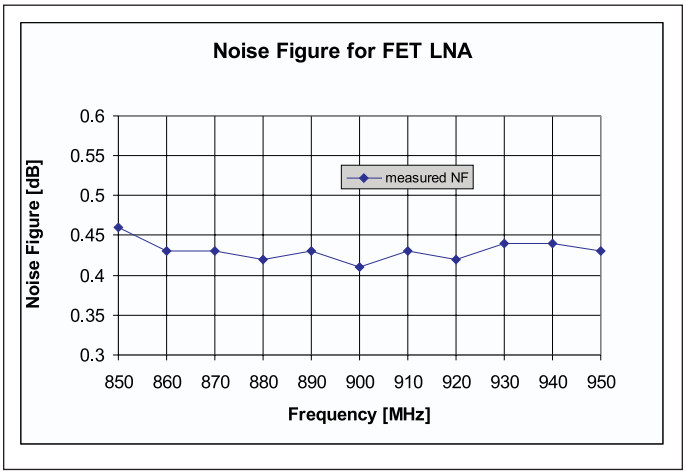
▲ **Figure 7a. Input return loss for the FET LNA.**



▲ **Figure 7b. Output return loss for the FET LNA.**



▲ **Figure 8a. Gain response for the FET LNA.**



▲ **Figure 8b. Noise figure for the FET LNA.**

article are all valid at much higher frequencies. Be aware that the effects of discontinuities and bends are greater at high frequencies where signal wavelengths are shorter. Synthesis software is available that will allow first time design success at X band and beyond [6]. Following the guidelines presented above will greatly assist in obtaining good correlation between design simulation and practical results. ■

Acknowledgement

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6. Information can be found at www.ampsa.com

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