Properties of low dielectric constant buildup materials containing micron sized hollow silica

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***Abstract*— Build-up substrate materials are high-performing specialty materials that consist of inorganic reinforcing particulates evenly dispersed throughout a continuous thermoset polymer matrix. Build-up materials are of critical importance in high density interconnect applications and often serve as the dielectric layer in multilayer circuitry including interposers, substrate packaging, and redistribution layers. Thermoset build-up materials benefit from low coefficients of thermal expansion, high reliability, and are available as thin dielectrics allowing for high density circuitry. Typically, high concentrations of ceramic particulate reinforcement are necessary to yield a low rate of thermal expansion. Solid particles of silica have the disadvantage of silica naturally raising the dielectric constant of a composite material relative to the low loss polymer resin which contributes to a lower dielectric constant. The future of build-up material requires increasingly lower loss for applications such as machine learning, AI, 5/6G, and high-speed switching. Although not as obvious as dissipation factor, there is also an advantage of lowering the dielectric constant. Increasing densification and finer lines and spaces leads to increasingly higher transmission line losses. Lower dielectric constant dielectrics allow a reduction in dielectric thickness while maintaining a given trace width. In order to meet the rapidly growing needs of increasingly higher density interconnect with the lowest losses, lower dielectric constant and lower dissipation factor build-up materials can be achieved by designing the thermoset matrix with lower dissipation factor and replacing solid particulates of silica with micron sized hollow silica, effectively taking advantage of air within the dielectric medium. In this study, we investigate the dielectric, mechanical and thermal properties of thermoset polymer buildup films that have been reinforced with hollow silica particulates.**

Keywords—buildup films, low dielectric constant, hollow silica.

I. INTRODUCTION

With the advent of 5/6G and wireless communication percolating into mainstream usage, the market for chip packing and HDI applications continues to rapidly grow. This ever-expanding market is driven by the increasingly stringent requirements of the semiconductor industry, with devices requiring higher density routing and finer pitch spacing than ever before. Build-up materials are thermoset polymer composites that serve as the dielectric layers in semiconductor packaging and HDI applications. The dielectric constant of the build-up film directly impacts signal propagation speed and transmission line loss. The use of low dielectric constant buildup materials can allow for a reduction in thickness while maintaining a given trace width, leading to lower transmission loss and higher density circuitry. Additionally, using low Dk buildup films may allow for higher signal speed, since propagation speed is inversely proportional to Dk. To therefore meet the exacting demands of the future chip packaging and HDI industry, lowering the Dk is but one critical piece of the puzzle.

Another important aspect in designing faster next generation buildup films is lowering the dissipation factor (Df). The Df measures signal attenuation as an electromagnetic wave propagates down a transmission medium and can thus be considered a measure of signal loss down a given transmission line. Both Df and Dk can be negatively affected by dielectric aging. Dielectric aging may be measured by measuring the change in Dk or Df as a function of time at elevated temperatures. For most hydrocarbon-based buildup films, Df steadily increases when exposed to prolonged periods of high temperature. While having a low Df is important in thermally static digital applications, for applications that require large fluctuations in temperature (such as avionics), it is imperative that the buildup film displays robust anti-aging properties and that the Dk and Df remain relatively low upon extended heat exposure.

In addition to anti-aging, it is also important for next generation buildup films to display robust thermal reliability. Coefficient of thermal expansion (CTE) is a measure of the dimensional change in a cured build-up film as a function of temperature and low CTE is directly correlated to microvia reliability and longevity. Resin flow and melt viscosity are other parameters to consider in designing next generation buildup films. With state-of-the-art assemblies for chip packaging becoming increasingly complex, the use of high flow and low viscosity resin systems allows for buildup films to fill copper artwork where copper may be plated as high as 1-2 mils.

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It is thereby important for next generation build-up materials to balance several important parameters to optimize performance, reliability, and processability. Conventional buildup films in today's market typically consist of fiber glass impregnated with resin and ceramic particulates. However, glass-based buildup films suffer from issues such as low resin flow through the weaves of fiberglass, which can lead to voiding and issues with filling the copper traces. The weave of the fiberglass also physically limits the dielectric thicknesses and microvia sizes achievable, which are becoming increasingly small as we move towards denser and more complex chip packaging. One solution to these issues is to use glass-free nonreinforced buildup films, consisting solely of resin and ceramic filler. Both the resin and the ceramic particulates influence the many properties including: dielectric properties such as DK/DF, adhesion, CTE, flow and fill, moisture absorption, etc. Filler materials in today's buildup films include ceramics such as silica (Dk = 3.8) and alumina (Dk = 9-10) and boast advantageous properties such as high temperature resistance, high hardness, and a low coefficient of thermal expansion. However, the dielectric constants of these materials may sometimes not be low enough for some next-generation packaging applications. In recent years, hollow silica particles (Dk = 1.2-2.0) have drawn attention as potential low Dk filler alternatives. Utilizing hollow silica effectively takes the advantage of air within the dielectric medium, lowering the dielectric constant, weight, and density of the buildup film.

Currently, 20-40 micron sized hollow particles are being commercially utilized in fiberglass reinforced composites such as AGC TLY-5 and MW-8300. However, there can be issues when using hollow fillers of this size. During microvia formation, if a drill bit partially drills into a hollow sphere, this may allow for copper plating chemistry, surfactants, low boiling point solvents, or other desmear or fabrication chemicals to become trapped in the hollow particle during the various fabrication steps (see Fig. 1). Then upon solder reflow, these trapped chemicals can outgas, leading to unwanted blistering and delamination. 20-40 micron sized hollow spheres are also deemed too large for chip packaging and high density circuitry applications, which require often require 25–50micron sized microvias and 75-100 micron spaces.

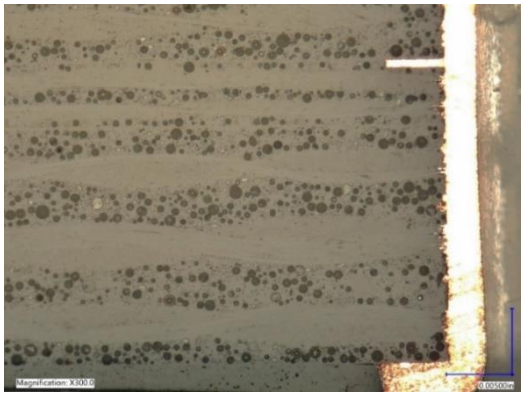

Figure 1: Magnified cross-sectional image of MeteorWave 8300. Copper can be seen filling hollow spheres on the plated through hole barrel wall.

One way to take advantage of the dielectric properties of hollow particles but avoid the aforementioned issues is to utilize smaller hollow spheres. In this study, we investigate the dielectric, mechanical and thermal properties of glass-free thermoset polymer buildup films based on fastRise™ resin systems that have been reinforced with varying concentrations of hollow and filled silica spherical particulates. We have investigated how incorporation of hollow silica impacts the dielectric constant, coefficient of thermal expansion, rheological profile and flow of the buildup film. Without disclosing proprietary information, we have also studied how simply changing the resin system of the buildup film (keeping all other factors constant) can drastically improve the dielectric aging properties. We have attempted to find an optimal balance of dielectric constant, CTE, flow and viscosity to meet the exacting demands of the future chip-packing industry. The results from this study will pave the way towards faster and more reliable buildup materials for high data rate signal transmission.

II. Methods

A. Sample Creation

Buildup films investigated in this study were based on fastRise™ resin systems and reinforced with varying loadings of hollow silica (D_{50} = 3 microns) and filled silica (D_{50} = 3 microns). Samples were created by dissolving resin components in 30 wt. % toluene, incorporating the appropriate type and amount of filler, and mixing using a high shear mixer. All samples were cast into thin films using Buschman™ drawdown bars, B-staged at 155 °C and fully cured at 230 °C for 2 hours at 100 psi.

B. Dielectric Measurements

Dk and Df was measured using a Split Post Dielectric Resonator (QWED Technologies) at 10 GHz with an Agilent Technologies N5230A PNA Series Network Analyzer. Aging measurements were done by keeping samples in a Class A Industrial Oven at 150 °C (non-vacuum conditions) and measuring the changes in Dk/Df over the course of 50 days.

C. Thermal Measurements

Dimensional change and CTE was measured using a Q400 Thermomechanical Analyzer (TA Instruments). Data was collected from -40 to 300 °C (two thermal cycles), CTE/dimensional change was calculated from the second thermal cycle.

D. Rheological Measurements

Rheological profiles were measured using an APA 2000 Rheometer (Alpha Technologies). Data was taken from 40-200 °C with a 2.5 mm gap width, 37 mm plate diameter, 100 cpm frequency, 0.050-degree strain, and 5 °C/minute heat rise.

E. Optical Measurements

SEM images were taken using a JSM-7100F (JEOL) Scanning Electron Microscopy at 5 kV accelerating voltage, 52 µA emission current, through a secondary electron detector.

III. RESULTS & DISCUSSION

A. Dielectric Properties of Buildup Film

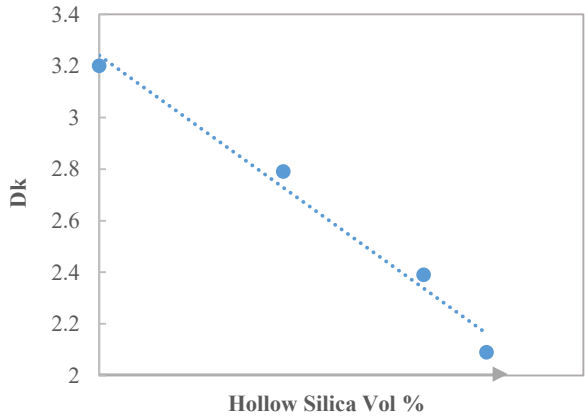

Figure 2: Dk of samples as a function of volume % hollow silica.

Fig. 2 shows the dielectric constant of the measured build-up film as a function of hollow silica volume %. Each sample altered the ratio of filled silica to hollow silica while keeping the overall resin to filler ratio constant. At 0 vol. % hollow silica/100 vol. % filled silica (control), the Dk of the buildup film is 3.2. Upon increasing the vol. % of hollow silica, the Dk drops in a linear fashion. At an appropriate combination of hollow silica and solid silica, the Dk was found to be ~ 2.09. These results indicate that incorporation of hollow silica may be an effective strategy to lower Dk of buildup films.

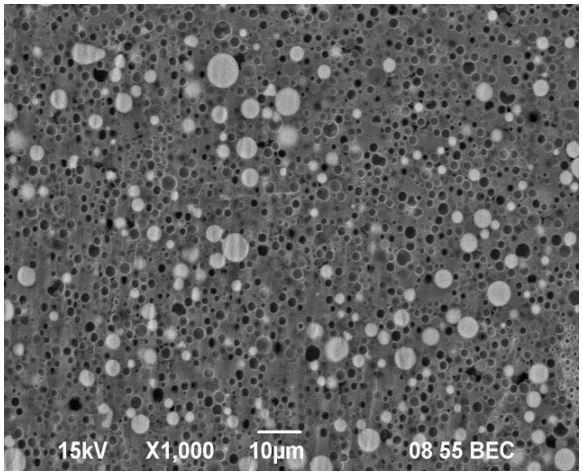

Figure 3: SEM image of buildup film containing 2-3 micron sized hollow silica and filled silica spherical particulates.

Fig. 3 shows an SEM image of the non-reinforced buildup film filled with 2-3 micron sized hollow and filled silica spheres.

B. Thermal Properties of Buildup Film

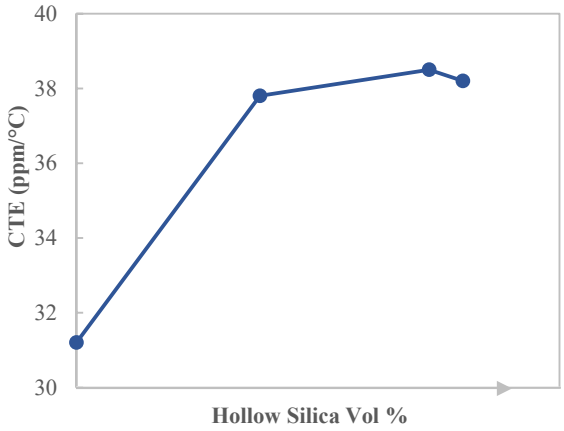

Figure 4: Coefficient of thermal expansion of buildup films containing hollow silica from 150-260 °C.

Fig. 4 shows the coefficient of thermal expansion (CTE) of the build-up film as a function of hollow silica volume %, from 150 °C to 260 °C. These temperatures were chosen to emulate solder refloat conditions done during fabrication and assembly processes. At 0 vol. % hollow silica/100 vol. % filled silica (control), CTE = 32 ppm/°C. Upon incorporation of hollow silica, the CTE increases to ~38 ppm/°C, which is still considered acceptable for many chip-packing applications. The CTE remains relatively consistent, even when using hollow silica in higher concentrations. The overall increase in CTE upon incorporation of hollow silica may be explained by the susceptibility of hollow filler materials to expand more under heat compared to filled silica, due to lower structural core support. Thickening the hollow silica wall may provide higher structural support and could potentially yield even lower CTE values.

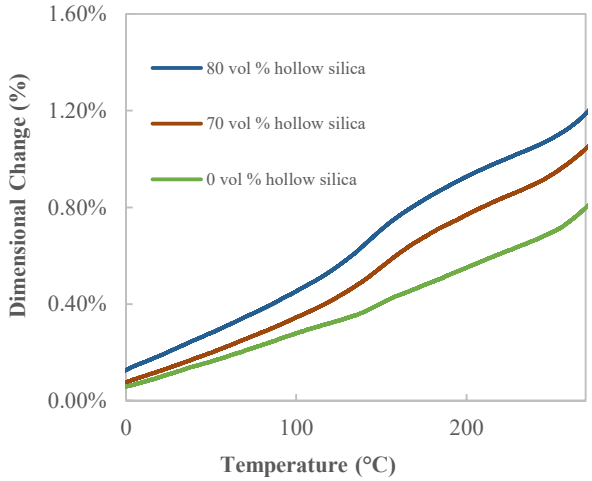

Figure 5: Temperature vs dimensional change of buildup film using hollow silica.

Fig. 5 shows the overall dimensional change of non-reinforced buildup films as a function of temperature for 0 vol. % hollow silica, 70 vol % hollow silica, and 80 vol % hollow silica. While dimensional change slightly increases upon addition of hollow silica, the trend remains linear for all samples studied. This trend contrasts with typical buildup films that display an exponential increase in dimensional change around the glass transition temperature of the film. The linear change in dimensional change further displays the unique thermal properties of these films, which will prove useful for high reliability applications.

C. *Rheology and Flow of Buildup Film*

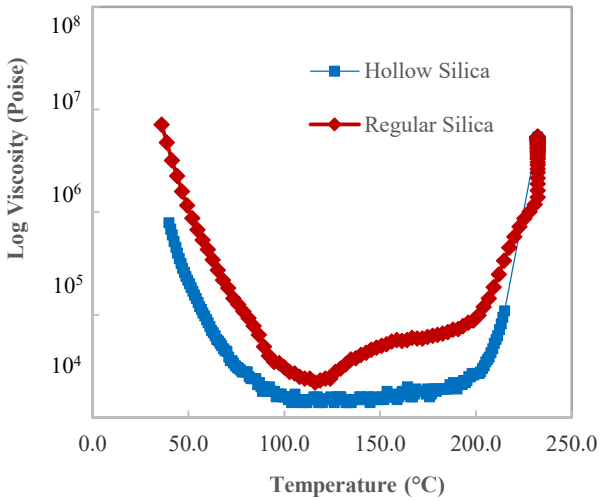

Figure 6: Viscosity curve of buildup film containing hollow silica

Fig. 6 shows the viscosity profile of buildup films containing just filled silica and that containing a combination of filled/hollow silica from 40 to 230 °C (taken at 5°C/minute heat rise). It should be noted that the hollow silica containing buildup film had a higher volume % of resin than the filled silica containing buildup film sample, which likely contributes to its lower viscosity. Nevertheless, by adjusting the formulation, it is possible to achieve a minimum melt viscosity as low as ~1.5 x 10^4 Poise and a wide processing window (~100-200 °C) using the hollow silica. It is possible to further modify the flow and viscosity of these build-up films by careful selection of the resin components or by controlling the overall ratio of resin to filler. Fig. 7 shows a cross-section image of the buildup film that was cured on top of a FR-4 laminate (160 °C for 2 hours at 400 psi). The top image is a glass-free buildup film that contains just filled silica, while the bottom image is a glass-free buildup film containing both filled and hollow silica. Both films seamlessly flow into the 15-mil spaces between the copper, indicating that using hollow silica may be suitable for next generation build-up film applications that require filling of thinner lines and spaces.

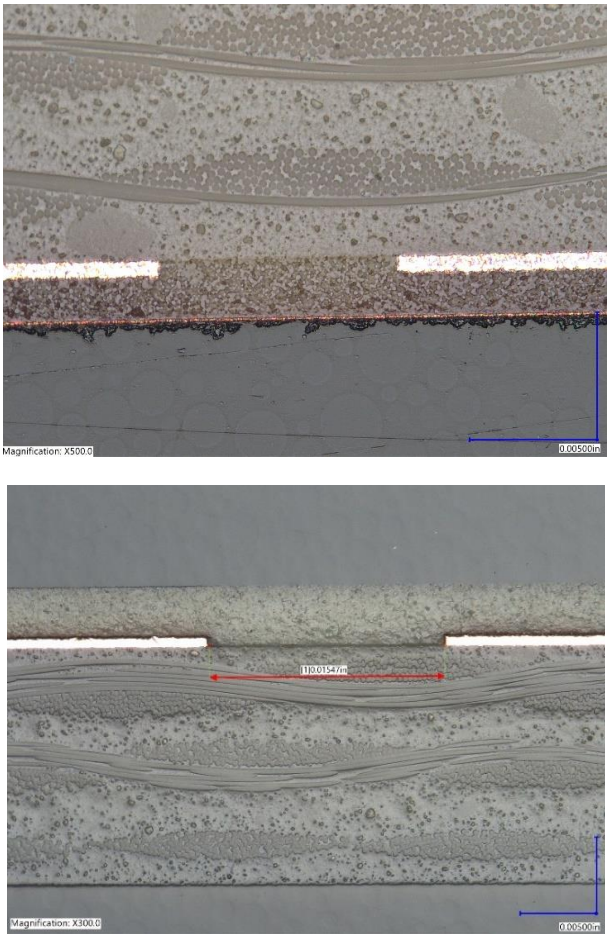

Figure 7: Top: Cross section image of non-reinforced silica containing buildup film cured on top of FR-4. Bottom: Cross section image of buildup film containing both silica and hollow silica particulates, cured on top of FR-4 laminate. In both cases, the buildup film can seamlessly fill between the copper traces, showcasing the film's ability to adequately flow between the copper traces.

D. *Dielectric Aging Properties*

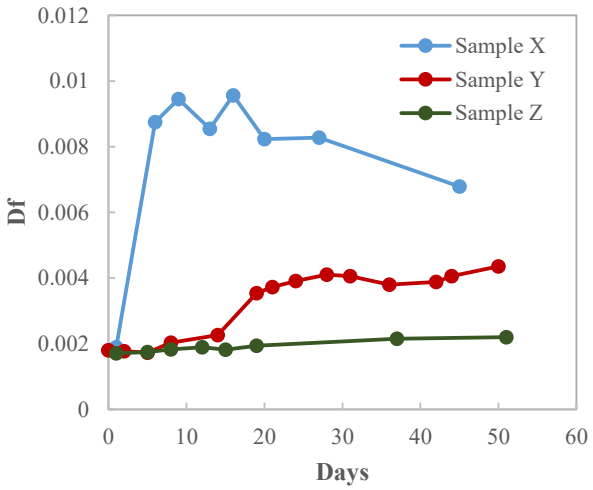

Figure 8: Dielectric aging properties of buildup film. Measured Df vs time at 150 °C

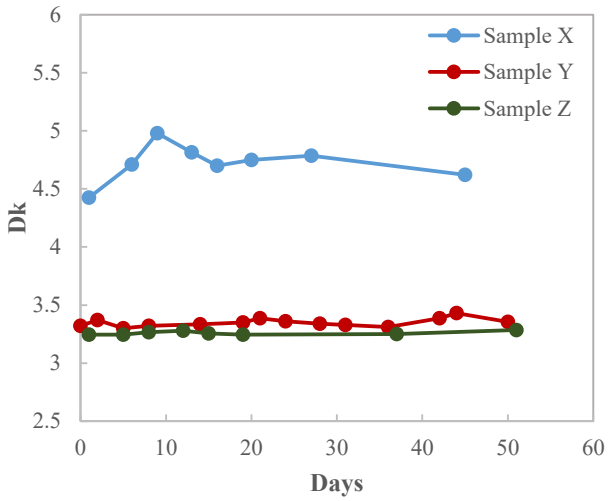

Figure 9: Dielectric aging properties of buildup film – Measured Dk vs time at 150 °C.

Fig. 8 shows the change in Df as a function time at 150 °C of the buildup film samples. While these samples contained only filled silica (no hollow silica), all samples had the same volume % of filler and resin; the only difference amongst the samples is the chemical composition of the resin used. Sample Z is the hydrocarbon-based resin system utilized in all hollow silica-containing samples studied in Sections A-C (Results and Discussion) of this paper. For comparative samples X and Y, Df steadily increases with time, with a 257% and 140% increase in Df by the end of the study. However, in sample Z, the Df remains relatively stable for the duration of the study with an overall % increase of 23%. After 51 days of aging at 150 °C, the final Df for Sample X is 0.0022, which still meets the exacting demands for dissipation factor in chip packaging and HDI applications.

Fig. 9 shows the dielectric aging of Dk as a function of time at 150 °C. For Sample X, the Dk increases by 4.5% by the end of the study while in Samples Y and Z, the Dk increases by just 1.2% by the end of the study. These results indicate that while Dk is also influenced the resin composition of the buildup film, it has a weaker impact on the overall dielectric aging compared to Df.

Table 1: Change in Df for samples X, Y, and Z from beginning to end of dielectric aging study.

Sample	Df, initial	Df, final	% Increase in Df
X	0.00190	0.00679	257%
Y	0.00181	0.00436	140%
Z	0.00171	0.00220	29%

Table 2: Change in Dk for samples X, Y, and Z from beginning to end of dielectric aging study.

Sample	Dk, initial	Dk, final	% Increase in Dk
X	4.43	4.62	4.5%
Y	3.36	3.32	1.2%
Z	3.29	3.25	1.2%

These results also highlight the importance of the polymer resin in achieving robust anti-aging properties for the buildup film. Whilst ceramic fillers remain relatively inert to oxidation, the organic nature of polymers make them conducive to the creation of free radicals under prolonged heat exposure. This is especially true in organic compounds that contain internal olefins such that are conducive to oxidation. Selecting resin systems that minimize these changes may be an important step in creating anti-aging buildup films. Combining the appropriate anti-aging resin system with the appropriate ceramic filler particulates can allow for creation of a buildup film with both low Dk and robust anti-aging properties that will meet the exacting future demands of extreme temperature applications like automotive or avionics applications. Table 1 shows the % change in Df while Table 2 shows the % change of Dk of the buildup films measured in this study.

IV. Conclusions

This paper investigated the dielectric, thermal, and rheological properties of buildup films using 2-3 micron sized hollow silica as a filler. It was found that increasing the ratio of hollow silica led to a linear decrease in the dielectric constant of the buildup film, and at a certain combination of hollow and filled silica, a Df of 2.09 can be achieved. These results imply that these buildup materials may be of use to certain next-generation chip packaging applications. It was also found that incorporating high loadings of hollow silica allowed for CTE values < 40 ppm/°C from 150-260 °C. Dimensional change as a function of temperature was surprisingly found to increase linearly, which contrasts with standard buildup films where dimensional change typically increases exponentially around the glass transition temperature. This linearity of expansion with temperature is a testament to the choice of resin materials and the nature of the crosslinking. In studying the rheological profile of the hollow silica containing buildup films, it was found that the minimum melt viscosity achievable was ~1.5 x 10^4 Poise and the buildup film had a processing window (100-200 °C). Viscosity can be further optimized and tailored by the proper balance of resin and filler amount and type. Optical microscopy images of the buildup films further corroborated material processability and showcased seamless flowability of the buildup films in between copper traces. Finally, changes in Dk and Df of the buildup films were monitored as a function of time at 150 °C in a dielectric aging study. It was found that while Dk remained relatively consistent throughout the study, the Df was susceptible to changes (likely from oxidation occurring in the resin system), but that these changes can be minimized by proper selection of the polymer resin. The results from this study imply that hollow silica spheres combined with the fastRise™ resin system may be suitable for next generation HDI and chip packaging solutions.

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REFERENCES

[1] Thomas McCarthy, Paul Cook, and Steve Schow, “HDI Build-up Layers for Reliability”, IPC APEX EXPO™ (2022).

[2] Thomas McCarthy and Steve Schow, “Using Low CTE Materials to Manufacture Reliable Stacked Microvia Structures”, IPC APEX EXPO™ (2023).

[3] Steve Schow, Bob Gosliak, Thomas McCarthy, “New Resin Systems Used to Solve Circuit Board Fabrication Issues”, IPC APEX EXPO™ (2023).

[4] Seung-Hyun Chae, Amit Nanjia, “Methodologies to Mitigate Chip-Package Interaction”, Electronic Design (2015).

[5] “AN 672: Transceiver Link Design Guildlines for High-Gbps Data Rate Transmission”, Altera Corporation (2020).

[6] Kella Knack, “The Increasingly Important Role of Dielectric Loss Tangent in PCB Laminates”, Altium (2020).

[7] Barry Thaler, Paul Bratt, “Properties of Low Dielectric Constant Laminates”, Empfasis (2010).